What is clamed is:

1. A analog to digital converter implemented in one chip, comprising:

an on-chip reference voltage generator for generating N number of reference voltages, N being a positive integer; and

a conversion means for converting the inputted analog signal into a digital signal by using the reference voltages.

2. The analog to digital converter as recited in claim 1, wherein the on-chip reference voltage generator includes a voltage level shifter for use in generating the reference voltages.

3. The analog to digital converter as recited in claim 1, further comprising M number of filters coupled between the on-chip reference voltage generator and the conversion means for removing a noise contained in the reference voltages, M being a positive integer.

4. The analog to digital converter as recited in claim 1, wherein the on-chip reference voltage generator includes:

an initial voltage generator for generating an initial voltage; and

a voltage level shifter for generating the reference voltages having N voltage levels by shifting a voltage level of the initial voltage.

5. The analog to digital converter as recited in claim 4, wherein the on-chip reference voltage generator includes a voltage driver for stabilizing the reference voltages.

6. The analog to digital converter as recited in claim 4, wherein the voltage level shifter includes:

a first voltage inducing block for receiving the initial voltage to generate an induced voltage;

a voltage shifting block for outputting the reference voltages by shifting a voltage level of the induced voltage as the voltage level of the initial voltage referenced on an operating current; and

a first driving block for generating the operating current to the voltage shifting block.

7. The analog to digital converter as recited in claim 6, wherein the voltage level shifter includes a first capacitor coupled between the voltage inducing block and the voltage dividing block for stabilizing the reference voltages.

8. The analog to digital converter as recited in claim 6, wherein the first voltage inducing block includes a differential amplifier for generating the induced voltage.

9. The analog to digital converter as recited in claim 6, wherein the first driving block includes a MOS transistor coupled to a supply voltage and the voltage dividing block,

its gate being coupled to the first voltage inducing block.

10. The analog to digital converter as recited in claim 6, wherein the voltage shifting block includes a plurality of resistors serially connected between the voltage driving block and a ground voltage.

11. The analog to digital converter as recited in claim 10, wherein the reference voltages are determined by the driving block and the voltage shifting block.

12. The analog to digital converter as recited in claim 11, wherein the reference voltages are divided into first and second reference voltages.

13. The analog to digital converter as recited in claim 11, wherein the voltage driver includes:

a first driving unit for stabilizing the first reference voltage; and

a second driving unit for stabilizing the second reference voltage.

14. The analog to digital converter as recited in claim 13, wherein the first driving unit includes:

a second voltage inducing block for receiving the first reference voltage to generating a first voltage;

a second driving block connected to a supply voltage for

stabilizing the first voltage to output the stabilized first voltage as the first reference voltage;

a second capacitor coupled between the second voltage inducing block and the second driving block for stabilizing the first voltage; and

a first resistor coupled between the second voltage inducing block and the second driving block for stabilizing the first reference voltage.

15. The analog to digital converter as recited in claim 14, wherein the second voltage inducing block includes a differential amplifier for generating the first voltage.

16. The analog to digital converter as recited in claim 13, wherein the second driving block includes a MOS transistor coupled to the supply voltage and the first resistor, its gate being coupled to the second voltage inducing block.

17. The analog to digital converter as recited in claim 16, wherein the second driving unit includes:

a third voltage inducing block for receiving the first reference voltage and inducing the second reference voltage;

a third driving block connected to a ground voltage for stabilizing the second reference voltage to output the stabilized second voltage as the second reference voltage;

a third capacitor coupled between the third voltage inducing block and the third driving block for stabilizing the

second reference voltage; and

a second resistor coupled between the third voltage inducing block and the third driving block for stabilizing the second reference voltage.

18. The analog to digital converter as recited in claim 17, wherein the third voltage inducing block includes

a differential amplifier for inducing the second reference voltage by a current mirror.

19. The analog to digital converter as recited in claim 18, wherein the second driving block includes

a MOS transistor coupled to the ground voltage and the first resistor, its gate being coupled to the third voltage inducing block.

20. The analog to digital converter as recited in claim 3, wherein the filter is a RC filter.

21. The analog to digital converter as recited in claim 20, wherein the RC filter includes a capacitor embodied by a MOS transistor, its gate being served as one side of the capacitor and its source, drain and body being served as the other side of the capacitor.

22. A system having one chip analog to digital converter, comprising:

an on-chip reference voltage generator contained in the analog to digital converter for generating N number of reference voltages, N being a positive integer; and

a conversion means contained in the analog to digital converter for converting the inputted analog signal into a digital signal by using the reference voltages.

23. The system as recited in claim 22, wherein the on-chip reference voltage generator includes a voltage level shifter for use in generating the reference voltages.

24. The system as recited in claim 22, further comprising M number of filters coupled between the on-chip reference voltage generator and the conversion means for removing a noise contained in the reference voltages, M being a positive integer.

25. The system as recited in claim 22, wherein the on-chip reference voltage generator includes:

an initial voltage generator for generating an initial voltage; and

a voltage level shifter for generating the reference voltages having N voltage levels by shifting a voltage level of the initial voltage.

26. The system as recited in claim 25, wherein the voltage level shifter includes:

a first voltage inducing block for receiving the initial voltage to generate an induced voltage;

a voltage shifting block for outputting the reference voltages by shifting a voltage level of the induced voltage as the voltage level of the initial voltage referenced on an operating current; and

a first driving block for generating the operating current to the voltage shifting block.

27. The system as recited in claim 26, wherein the voltage shifting block includes a plurality of resistors serially connected between the voltage driving block and a ground voltage.

28. The system as recited in claim 27, wherein the filter is a RC filter.

29. The system as recited in claim 28, wherein the RC filter includes a capacitor embodied by a MOS transistor, its gate being served as one side of the capacitor and its source, drain and body being served as the other side of the capacitor.